IN THE CLAIMS:

Please amend claims 1-18 as provided below.

1. (currently amended) A device ~~(1)~~ for calculating feedback signaling message (FSM) bits ~~(FSM(s))~~ by means of which the signals sent from two antennas of a base station are influenced with reference to their phase difference and/or their amplitudes with the aid of two estimated channel impulse responses ~~(h1,n(s), h2,n(s))~~,

[[-]] wherein the device ~~(1) being present~~ is in hard-wired form, and wherein the device

[[-]] is configured to generate a complex phasor ~~(H21) being formed~~ from components ~~(h1,n(s), h2,n(s))~~ of the two channel impulse responses, and further configured to produce

[[-]] an FSM bit ~~(FSM(s)) being produced by means of~~ by a rotation and projection of the phasor ~~(H21) and, in particular, of~~ and a comparison of the rotated and projected phasor with a threshold value ~~value decision~~.

2. (currently amended) The device ~~(1)~~ as claimed in claim 1, ~~characterized~~

~~in that~~ wherein the components ~~(h1,n(s), h2,n(s))~~ of the two channel impulse responses ~~can be~~ are applied at inputs ~~(In1, ..., In4)~~ of the device ~~(1)~~, and wherein

~~in that~~ control signals ~~(C1,k(s), ..., C6,k(s)) can be~~ are applied at control inputs ~~(Config1, ..., Config6)~~ of the device ~~(1)~~, and wherein

~~in that~~ the FSM bit ~~(FSM(s)) can be tapped~~ is provided at an output of the device ~~(1)~~, the FSM bit ~~(FSM(s))~~ being calculated as a function of the components ~~(h1,n(s), h2,n(s))~~ of the two channel impulse responses and the control signals ~~(C1,k(s), ..., C6,k(s))~~.

3. (currently amended) The device ~~(1)~~ as claimed in claim 2, ~~characterized by~~

~~by~~ wherein the device comprises a logic unit ~~(2, 3)~~ configure to receive and selectively arrange the two channel impulse responses, and a processing unit ~~(4, ..., 9)~~ connected downstream of the logic unit configured to process the two channel impulse responses based on the selective arrangement thereof ~~(2, 3)~~.

4. (currently amended) The device ~~(1)~~ as claimed in claim ~~1~~3, ~~characterized~~

~~in that~~ wherein the components ~~(h1,n(s), h2,n(s))~~ of the two channel impulse responses are present at inputs ~~(In1, In2, In3, In4)~~ of the logic unit ~~(2, 3)~~, wherein

~~in that~~ the logic unit ~~(2, 3)~~ has outputs ~~(Out1, Out2, Out5, Out6)~~ whose number is equal to the number of its inputs ~~(In1, In2, In3, In4)~~, and wherein

~~in that~~ the inputs ~~(In1, In2, In3, In4)~~ of the logic unit ~~(2, 3) can be~~ are connected to the outputs ~~(Out1, Out2, Out5, Out6)~~ of the logic unit ~~(2, 3)~~ as a function of at least one of the control signals ~~(C1,k(s), ..., C5,k(s))~~.

5. (currently amended) The device ~~(1)~~ as claimed in claim 3 ~~or 4~~, ~~characterized~~

~~in that~~ wherein the processing unit comprises a multiplier stage ~~(4, 5)~~, an adder ~~(6)~~, a weighting stage ~~(7)~~, an accumulator ~~(8)~~ and a threshold value ~~value~~ decision unit ~~(9) are~~ connected in series in the prescribed sequence ~~in the processing unit (4, ..., 9)~~.

6. (currently amended) The device ~~(1)~~ as claimed in claim 5, ~~characterized~~

~~in that~~ wherein the multiplier stage has two multipliers ~~(4, 5)~~ whose inputs are connected in each case to two outputs ~~(Out1, Out2, Out5, Out6)~~ of the logic unit ~~(2, 3)~~, and wherein

~~in that~~ the inputs of the adder ~~(6)~~ are connected to the outputs of the multipliers ~~(4, 5)~~.

7. (currently amended) The device ~~(1)~~ as claimed in claim[[s]] ~~5 and~~ 6, ~~characterized~~

~~in that~~ further comprising a control signal ~~(C6,k(s)) is present at~~ coupled as an input to the weighting stage ~~(7)~~, and

~~in that~~ wherein the weighting stage ~~(7) applies~~ is configured to apply a weighting factor to ~~the~~ a sum ~~(Sk)~~ formed by the adder ~~(6), doing so~~ as a function of the control signal coupled thereto~~(C6,k(s)) present at it~~.

8. (currently amended) The device ~~(1)~~ as claimed in ~~one or more of~~ claim[[s]] 2 ~~to 7~~, ~~characterized~~

~~in that~~ wherein the control signals are stored in the form of control bits ~~(C1,k(s), ..., C6,k(s))~~ in a read-only memory.

9. (currently amended) The device ~~(1)~~ as claimed in ~~one or more of the preceding claims, characterized~~

~~in that~~ claim 1, wherein the device ~~(1)~~ is designed for the UMTS standard.

10. (currently amended) The device ~~(1)~~ as claimed in claim 9, ~~characterized~~

~~in that~~ wherein the control signals ~~(C1,k(s), ..., C6,k(s))~~ are a function of the slot number ~~(s)~~ of the FSM bit ~~(FSM(s))~~ to be calculated, and of ~~the~~ a CLTD mode.

11. (currently amended) The device ~~(1)~~ as claimed in claim ~~9 or~~ 10, ~~characterized~~

~~in that~~ wherein the control signals ~~(C1,k(s), ..., C6,k(s))~~ are a function of whether the slot number ~~(s)~~ of the FSM bit ~~(FSM(s))~~ to be calculated is an even or odd number.

12. (currently amended) A mobile radio terminal having a device ~~(1)~~ as claimed in ~~one or more of the preceding~~ claim[[s]] 1.

13. (currently amended) A method for calculating FSM bits ~~(FSM(s))~~ by means of which the signals sent from two antennas of a base station are influenced with reference to their phase difference and/or their amplitudes with the aid of two estimated channel impulse responses ~~(h1,n(s), h2,n(s)), having the following steps~~comprising:

(a) producing a complex phasor ~~(H21)~~ from components ~~(h1,n(s), h2,n(s))~~ of the two channel impulse responses; and

(b) calculating an FSM bit ~~(FSM(s))~~ by rotation and projection of the phasor ~~(H21)~~.

14. (currently amended) The method as claimed in claim 13, ~~characterized in that~~ wherein the rotation and projection of the phasor ~~(H21)~~ is determined by control signals ~~(C1,k(s), ..., C6,k(s))~~.

15. (currently amended) The method as claimed in claim 13 ~~or 14, characterized in that~~ wherein calculating the FSM bit comprises performing a threshold value ~~value decision is carried out~~ comparison after the rotation and projection of the phasor ~~(H21) in order to calculate the FSM bit (FSM(s))~~.

16. (currently amended) The method as claimed in ~~one or more of claims 13 to 15, characterized in that~~ claim 14, wherein the method is designed for the UMTS standard.

17. (currently amended) The method as claimed in claims ~~14 and~~ 16, ~~characterized~~

~~in that~~ wherein the control signals ~~(C1,k(s), ..., C6,k(s))~~ are a function of the slot number ~~(s)~~ of the FSM bit ~~(FSM(s))~~ to be calculated, and of ~~the~~ a CLTD mode.

18. (currently amended) The method as claimed in claim 17, ~~characterized~~

~~in that~~ wherein the control signals ~~(C1,k(s), ..., C6,k(s))~~ are a function of whether the slot number ~~(s)~~ of the FSM bit ~~(FSM(s))~~ to be calculated is an even or odd number.